Amendments to the Specification:

1) page 6, second paragraph, please replace this paragraph with the following amended text:

Fig. 1 shows a cross section of a semiconductor surface on the surface of which a contact pad has been created, the semiconductor surface is covered with a patterned layer of passivation,

Fig. 2 shows the cross section of Fig. 1 after a patterned layer of dielectric and a layer of metal have been created on the semiconductor surface,

Fig. 3 shows a cross section of Fig. 2 after a layer of interconnect metal and a layer of solder compound have been selectively deposited, and

Fig. 4 shows a cross section after ~~excessive~~ excess layers have been removed from the semiconductor surface and after the solder has been flowed, forming the interconnect bump.

2) page 6, last paragraph, page 7, first paragraph, please replace this paragraph with the following amended text:

Figs. 5 through 12 show the process of the invention, ~~s~~ as follows:

Fig. 5 shows a cross section of a semiconductor surface on the surface of which a contact pad has been created, the semiconductor surface is covered with a layer of passivation, a layer of UBM has been deposited.

3) page 8, first paragraph, please replace this paragraph with the following amended text:

Figs. 13 and 14 show a prior art ~~creation of a~~ solder bump, ~~for the purposes of~~ highlighting problems that are typically experienced in creating such a solder bump.

4) page 8, last paragraph, page 9, first paragraph, please replace this paragraph with the following amended text:

Fig. 1 shows an example of one of the conventional methods that can be used to create an interconnect bump.

A semiconductor surface 10 has been provided with a metal contact pad 14, the semiconductor surface 10 is protected with a layer 12 of passivation. An opening 11 has been created in the

layer 12 of passivation, the surface of the metal contact pad 14 is exposed through this opening 11.

Next, as shown in the cross section of Fig. 2, a dielectric layer 16 is deposited over the surface of the layer 12 of passivation. The layer 16 of dielectric is patterned and etched, creating an opening 13 in the layer 16 of dielectric that aligns with the metal pad 14 and that exposes the surface of the metal pad 14.

A layer of 18 of metal, also shown in the cross section of Fig. 2, typically created by applying Under Bump Metallurgy (UBM), is ~~created~~ deposited over the layer 16 of dielectric, this layer 18 of metal is in contact with the surface of the metal pad 14 inside opening 13. The layer 18 of metal that is above the metal pad 14 will, at a later point in the process, form a pedestal over which an interconnect bump will be formed.

This pedestal can ~~be~~ further be extended in height by the deposition and patterning of one or more additional layers (underlying the pedestal 18 shown in the cross section of Fig. 2) that may contain a photoresist or a dielectric material. These additional layers have not been shown in Fig. 2 but essentially have the shape of layer 16 and can be removed during

one of the final processing steps that are applied for the formation of the interconnect bump.

5) page 14, first and second paragraph, please replace this paragraph with the following amended text:

In-situ sputter clean has been performed of the exposed surface of the contact pad 14. A seed layer (not shown in Fig. 5) has been blanket deposited over the surface of the layer 12 of passivation, including the exposed surface of the contact pad 14, a film 18 of Under Ball Metallurgy has been blanket deposited over the seed layer.

~~Layer 10 is the surface of a semiconductor layer, a contact pad 14 has been created on surface 10. Surface 10 will typically be the surface of a semiconductor substrate, the surface of an interconnect substrate and the like. A contact pad 14 has been created on surface 10, electrical contact must be established with contact pad 14 by means of an overlying solder bump. Contact pad 14 serves as interface between the solder bump and electrical interconnects that are provided in the surface of layer 10.~~

~~Contact pad 14 can include a contact pad that is formed on a surface other than the surface of a substrate, such as the~~

~~surface of a printed circuit boards, flex circuits or a metallized or glass substrate or semiconductor device mounting support.~~

6) page 14, last paragraph, page 15, first paragraph, please remove this paragraph:

~~A layer 12 of passivation that may, for instance, contain Plasma Enhanced silicon nitride (PE Si_3N_4), is deposited over the surface of layer 10 and of contact pad 14. Layer 12 of passivation material may also have been created using successive and overlying depositions of layers of passivation material. The passivation layer 12 deposited over the surface of the semiconductor surface comprises a plurality of passivation layers. The plurality of passivation layers may be selected from such materials as PE Si_3N_4, SiO_2 and a photosensitive polyimide and phosphorous doped silicon dioxide and titanium nitride.~~

7) page 18, second paragraph, please replace this paragraph with the following amended text:

Layer 12 of passivation ~~layer~~ material, deposited over the ~~surface of said~~ semiconductor surface 10, can also comprise a

plurality of passivation layers, ~~this to provide~~ providing improved protection to underlying surfaces. This plurality of passivation layers can for instance be selected from a group comprising PE Si_3N_4, SiO_2, a photosensitive polyimide, phosphorous doped silicon dioxide and titanium nitride.

8) page 18, fourth paragraph, please replace this paragraph with the following amended text:

For ~~the~~ an in-situ sputter clean of the exposed surface of contact pad 14, a sputter ion-milling tool can be used, ~~using~~ applying Ar mixed with H_2 as a cleaning agent (sputter source).

9) page 20, fourth paragraph, please replace this paragraph with the following amended text:

Fig. 7 shows a cross section during the exposure of the layer 31 of photoresist. Exposure mask 32 is used for this ~~purposed of~~ exposure, on the surface of quartz substrate 34 of mask 32 are two concentric patterns 33 (a first pattern) and 36 (a second pattern) of opaque material, making mask 32 a grey-tone mask.

10) page 22, second paragraph, please replace this paragraph with the following amended text:

The reasons that the T-shape of the created layer 41 is of benefit can be explained as follows~~: if~~. If the surface area of the patterned layer of UBM is larger than the surface area of the contact pad, ~~the die crack will~~ die cracks 43, shown in the cross section of Fig. 13, are likely to occur between the solder bump 42 and the underlying layer 18 of UBM. By limiting the size of the surface area of the layer of UBM to the same size as the size the surface area of the contact pad, cracking ~~is~~ can be prevented ~~as has been shown in the cross section of Fig. 14~~. However, limiting the ~~size~~ the surface area of the patterned layer of UBM layer underlying the solder bump leads to limiting the size of the solder bump~~, see Fig. 15~~. By therefore creating a T-shaped solder form, more solder can be deposited, thereby creating ~~s~~ a larger solder bump without creating a layer of UBM as the footprint of the solder bump.

11) page 1, the title of the invention, please replace the title ~~NOVEL METHOD TO IMPROVE BUMP RELIABILITY FOR FLIP CHIP DEVICE~~ with the new title METHOD FOR IMPROVING BUMP RELIABILITY FOR FLIP CHIP DEVICES